Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A memory device comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored digital data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column and including a second circuit to test a level of stored digital data in the redundant memory cells; and

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver.

2. (currently amended) ~~The~~ A memory device ~~of claim 1~~ comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column and including a second circuit to test a level of stored data in the redundant memory cells; and

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver,

wherein the first circuit tests a voltage level of the stored data on a bitline coupled to one of said columns of memory cells.

3. (Original) The memory device of claim 2 wherein each of the memory cells comprises a transistor having a source, gate, and drain terminals, a first bias voltage is applied to a gate, a second bias voltage is applied to a source of said transistor, and a bias current flowing between the source and drain terminals of said transistor being independent of the data stored in said memory cell.

4. (Original) The memory device of claim 2, wherein the first circuit tests a current on a bitline coupled to one of said columns of memory cells, the current being indicative of and dependent on data stored in said memory cell.

5. (Original) The memory device of claim 4, wherein each of the memory cells comprises a transistor having a source, gate, and drain terminals, a low voltage is applied to the source, a bias voltage is applied to a gate, and a load is coupled to the drain, the current level is determined from the voltage on said load.

6. (Original) The memory device of claim 1 wherein said first and redundant y-drivers each comprise a pattern indicator circuit that comprises a NAND gate to generate an input data pattern indicator in response to input data applied thereto.

7. (Original) The memory device of claim 1 wherein each of said first and redundant y-drivers further comprise a pattern indicator circuit to generate an input data pattern indicator in response to received input data.

8. (Original) The memory device of claim 7 wherein the input data received substitutes a predetermined data value and said substitution prevented by said disable signal generated by said controller.

9. (Original) The memory device of claim 7 wherein the input data pattern indicator inhibits the first y-driver from programming the memory cell in response to a predetermined data value.

10. (currently amended) ~~The~~ A memory device ~~of claim 7~~ comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column and including a second circuit to test a level of stored data in the redundant memory cells; and

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver,

wherein each of said first and redundant y-drivers further comprise a pattern indicator circuit to generate an input data pattern indicator in response to receive input data,

the memory device further comprising a status latch responsive both to said pattern indicator circuit and to said controller.

11. (Original) The memory device of claim 10 wherein said status latch controls inhibiting the first and redundant y-drivers from programming the memory cell in response to a predetermined data value.

12. (Original) The memory device of claim 10 further comprising a status flag circuit indicative of the outcome of data read or program operations, said status flag circuit being coupled to said controller.

13. (Original) The memory device of claim 12 wherein said status flag circuit is enabled by said status latch and disabled in response to a predetermined data value or disabled in response to said disable signal generated by said controller.

14. (currently amended) ~~The~~ A memory device ~~of claim 1~~ comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column and including a second circuit to test a level of stored data in the redundant memory cells; and

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver,

wherein the first circuit includes a comparator having a first input coupled to a reference line for receiving a reference level, having a second input coupled to a data bit line for detecting stored data level, the comparator autozeroing any offset of said comparator before comparison of the reference level and the stored data level.

15. (Original) The memory device of claim 1 further comprising a storage circuit for storing addresses of memory cells failing said testing of voltage level of stored data, and wherein said controller generates said selection and disable signals in response to a match between one of the said stored addresses and an applied address signal.

16. (Original) The memory device of claim 15 wherein the storage circuit includes a fuse circuit.

17. (Original) The memory device of claim 15 further comprising an address sequencer to address the storage circuit to read stored addresses of failing memory cells.

18. (Original) The memory device of claim 17 further comprising an address sequencer to read all storage locations of the storage circuit for stored addresses of said failing memory cells.

19. (Original) The memory device of claim 15 further comprising an address sequencer to read the locations of the storage circuit having stored addresses of said failing memory cells.

20. (Original) The memory device of claim 1 further comprising:

an address sequencer coupled to the controller, the plurality of first y-drivers, and the plurality of redundant y-drivers for generating address signals to address said first y-drivers or redundant y-drivers.

21. (currently amended) ~~The~~ A memory device ~~of claim 17~~comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column and including a second circuit to test a level of stored data in the redundant memory cells; and

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver,

a storage circuit for storing addresses of memory cells failing said testing of voltage level of stored data, and wherein said controller generates said selection and disable signals in response to a match between one of the said stored addresses and an applied address signal; and

an address sequencer to address the storage circuit to read stored addresses of failing memory cells, wherein the address sequencer further generates address signals for said defective columns and does not generate address signals for other ones of said columns.

22. (currently amended) ~~The~~ A memory device ~~of claim 17~~comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column and including a second circuit to test a level of stored data in the redundant memory cells; and

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver,

a storage circuit for storing addresses of memory cells failing said testing of voltage level of stored data, and wherein said controller generates said selection and disable signals in response to a match between one of the said stored addresses and an applied address signal; and

an address sequencer to address the storage circuit to read stored addresses of failing memory cells,

wherein the address sequencer generates said address signals in a predetermined timing relationship with the generation of the selection signal and the disable signal.

23. (Original) The memory device of claim 22 wherein the predetermined timing relationship is a real time relationship.

24. (currently amended) ~~The~~ A memory device ~~of claim 17~~comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column and including a second circuit to test a level of stored data in the redundant memory cells; and

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver,

a storage circuit for storing addresses of memory cells failing said testing of voltage level of stored data, and wherein said controller generates said selection and disable signals in response to a match between one of the said stored addresses and an applied address signal; and

an address sequencer to address the storage circuit to read stored addresses of failing memory cells,

wherein the address sequencer generates the address and the first y-drivers and the redundant y-drivers decode in the address in a time less than the reading of the memory cells.

25. (currently amended) ~~The~~ A memory device ~~of claim 17~~ comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column and including a second circuit to test a level of stored data in the redundant memory cells; and

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver,

a storage circuit for storing addresses of memory cells failing said testing of voltage level of stored data, and wherein said controller generates said selection and disable signals in response to a match between one of the said stored addresses and an applied address signal; and

an address sequencer to address the storage circuit to read stored addresses of failing memory cells,

wherein the address sequencer generates addresses associated with an address of each column of redundant memory cells.

26. (currently amended) ~~The~~ A memory device ~~of claim 17~~ comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column and including a second circuit to test a level of stored data in the redundant memory cells; and

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver,

a storage circuit for storing addresses of memory cells failing sub testing of voltage levels of stored data, and wherein said controller generates said selection disable signals in response to a match between one of the said stored addresses and an applied address signals; and

an address sequence to address storage circuit to read stored addresses of failing memory cells, wherein the address sequencer generates addresses associated with an address for each column of redundant memory cells that is enabled and does not generate an address for said columns of redundant memory cells that are not enabled.

27. (Original) The memory device of claim 1 wherein the plurality of redundant y-drivers are substantially the same as the first y-drivers and are controlled by an enable signal.

28. (currently amended) ~~The~~ A memory device ~~of claim 27~~ comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column and including a second circuit to test a level of stored data in the redundant memory cells; and

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver,

wherein the plurality of redundant y-drivers are substantially the same as the first y-drivers and are controlled by an enable signal,

wherein the enable signal is responsive to said controller.

29. (currently amended) ~~The~~ A memory device ~~of claim 1~~ comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column and including a second circuit to test a level of stored data in the redundant memory cells; and

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver,

wherein the plurality of memory cells of said first memory array and said redundant memory array are further arranged in a plurality of pages, each column of said plurality of columns being associated with a corresponding page.

30. (currently amended) ~~The~~ A memory device ~~of claim 1~~ comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column and including a second circuit to test a level of stored data in the redundant memory cells; and

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver,

wherein said selection and disable signals from said controller are operable upon a group of said redundant and first y-drivers respectively, said group addressed by the smallest address operable by said memory device.

31. (currently amended) ~~The~~ A memory device ~~of claim 1~~ comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column and including a second circuit to test a level of stored data in the redundant memory cells; and

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver,

wherein the first memory array is arranged in segments of memory cells, and the controller generates a selection signal for said redundant memory array and generates a disable signal to disable a segment corresponding to a memory cell failing said testing.

32. (currently amended) ~~The~~ A memory device ~~of claim 15~~ comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant

memory cells in said column and including a second circuit to test a level of stored data in the redundant memory cells;

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver, and

a storage circuit for storing addresses of memory cells failing said testing of voltage level of stored data, and wherein said controller generates said selection and disable signals in response to a match between one of the said stored addresses and an applied address signal,

wherein the storage circuit comprises a plurality of fuse sets associated with the redundant memory cells, a number of said fuse set is less than the number of columns of redundant memory cells.

33. (currently amended) ~~The~~ A memory device ~~of claim 1~~ comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column and including a second circuit to test a level of stored data in the redundant memory cells; and

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver;

~~further comprising~~ a plurality of fuse sets storing addresses of some memory cells and wherein said fuse set comprises first and second fuse elements, and

a latch coupled to the first and second fuse elements for storing the contents of the first and second fuse elements, the first and second fuse elements and the latch being arranged as a differential amplifier.

34. (Original) The memory device of claim 33 wherein the memory cells comprise flash transistors, the columns of memory cells arranged in rows and columns, so that a predetermined number of memory cells form a fuse element, and the memory device further comprises at least one dummy row and at least one dummy column of memory cells.

35. (Original) The memory device of claim 34 wherein the two cells of each fuse element are disposed on a top portion and a bottom portion, respectively.

36. (Original) The memory device of claim 35 wherein one of said at least one dummy rows is disposed on said top portion, another one of said at least one dummy rows is disposed on said bottom portion, one of said at least one dummy column is disposed on a first side portion, and another one of said at least one dummy column is disposed on a second side portion opposite said first side portion.

37. (Original) The memory device of claim 36 wherein others of the dummy rows comprise floating connections.

38. (Original) The memory device of claim 35 wherein the column coupled to the bit line does not contact said memory cells except where the memory cells in said column coupled to the bit line are coupled to one of said plurality of fuse sets.

39. (Original) The memory device of claim 33 further wherein said fuse set couples to said controller, said controller being responsive to data stored in said fuse set.

40. (Original) The memory device of claim 34 wherein the predetermined number of memory cells forming said fuse element is two.

41. (Original) The memory device of claim 34 wherein the predetermined number of memory cells forming said fuse element is greater than two.

42. (Original) The memory device of claim 34 wherein the predetermined number of memory cells forming said fuse element is three, four or five.

43. (currently amended) ~~The~~ A memory device ~~of claim 1~~ comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column and including a second circuit to test a level of stored data in the redundant memory cells; and

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver; and

~~further comprising:~~ a second memory array including a plurality of second memory cells arranged in columns and for storing an extension and further including an extension y-driver coupled to a corresponding one of a plurality of said columns of second memory cells to read contents of second memory cells in said columns, and including a third circuit for testing a level of stored data in the second memory cells,

wherein said controller generates said selection signal to enable use of said redundant memory arrays and to generate a second disable signal to disable a portion of the second memory array of said data.

44. (currently amended) ~~The~~ A memory device ~~of claim 1~~ comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column and including a second circuit to test a level of stored data in the redundant memory cells; and

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver,

wherein data output is multiplexed at the output of the first y-drivers and the redundant y-drivers.

45. (currently amended) ~~The~~ A memory device ~~of claim 1~~ comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column and including a second circuit to test a level of stored data in the redundant memory cells; and

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver,

wherein output data is multiplexed at an input/output buffer.

46. (currently amended) ~~The~~ A memory device ~~of claim 1~~ comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column and including a second circuit to test a level of stored data in the redundant memory cells; and

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver,

wherein the first and redundant y-drivers comprise an inhibit circuit coupled to a bit line connecting a corresponding one of said plurality of columns of said memory cells to provide an inhibit voltage on said bit line.

47. (Original) The memory device of claim 46 wherein the inhibit circuit is a PMOS device.

48. (Original) The memory device of claim 46 wherein the inhibit circuit to provide said inhibit voltage on said bit line in response to the first circuit detecting a failure of the level of stored data in the memory cells.

49. (Original) The memory device of claim 46 wherein the voltage inhibit circuit provides said inhibit voltage on said bit line in response to a predetermined data value.

50. (currently amended) ~~The~~ A memory device ~~of claim 1~~ comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column and including a second circuit to test a level of stored data in the redundant memory cells; and

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver,

wherein the plurality of memory cells in the first memory array are further arranged in a plurality of pages, each page comprising groups of said columns, the controller generating said disable signal to prevent programming of a portion of one page of said first memory array in response to a predetermined data signal and enable another portion of said page to allow programming of said another portion.

51. (currently amended) ~~The~~ A memory device ~~of claim 1~~ comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column and including a second circuit to test a level of stored data in the redundant memory cells; and

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver; and

~~further comprising~~ a monitoring circuit coupled to a bit line coupling a column of memory cells.

52. (currently amended) ~~The~~ A memory device ~~of claim 1~~ comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column and including a second circuit to test a level of stored data in the redundant memory cells; and

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver,

wherein the memory device and cells are capable of storing N bits of multilevel data per memory cell.

53. (Original) The memory device of claim 52 wherein the controller generates the selection signal to enable selected redundant memory cells of one of said columns of said redundant memory array and generates the disable signal to disable corresponding memory cells of one of said columns of said first memory array in response to the failure of said testing of said voltage level, N being an optional number of bits capable of being stored per memory cell when there is no failure of said testing.

54 - 97. (cancelled).